WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

a target element; and

a metal fence provided so as to surround the target element,

the metal fence including (i) a lamination of metal wire layers for forming an electromagnetic isolation structure and (ii) a plurality of vias for connecting the metal wire layers with each other,

the metal fence satisfying

$d \leq \lambda/8$,

$WF \geq 5\delta$, and

$L \leq \lambda/20$,

where δ is a skin depth of an electromagnetic wave, c is a velocity of light, f is an operating frequency of the integrated circuit, d is a lateral-direction size of a metal-fence region, WF is a surrounding-line width of the metal fence, L is an interval between the vias, and $\lambda=c/f$ is a wavelength of a signal.

2. An integrated circuit as set forth in claim 1, further comprising:

a guard ring provided right under the metal fence, the guard ring being made of a first diffusion layer whose conductivity type is identical to a conductivity type of a

substrate,

the guard ring being connected with a fixed potential,

the guard ring being electrically isolated from the metal fence.

3. An integrated circuit as set forth in claim 1, further comprising:

a well provided below the target element, the well being connected with a substrate.

4. An integrated circuit as set forth in claim 1, further comprising:

a low-resistance layer provided below the target element, a conductivity type of the low-resistance layer being identical to a conductivity type of a substrate,

the low-resistance layer being connected with a fixed potential,

the low-resistance layer being electrically isolated from the metal fence.

5. The integrated circuit as set forth in claim 4, wherein:

an area of the low-resistance layer is equivalent to an area surrounded by the metal fence.

6. The integrated circuit as set forth in claim 5, wherein:

the low-resistance layer is a salicide diffusion layer.

7. The integrated circuit as set forth in claim 5, wherein:

the low-resistance layer is a silicidized polysilicon layer.

8. The integrated circuit as set forth in claim 1, wherein:

between a plurality of elements each of which has the metal fence is a substrate.

9. The integrated circuit as set forth in claim 1, wherein:

between an element having the metal fence and another element having no metal fence is a substrate.

10. The integrated circuit as set forth in claim 1, wherein:

the target element is an element that generates an electromagnetic field in the integrated circuit.

11. The integrated circuit as set forth in claim 10,

wherein:

the target element is a high-frequency device.

12. The integrated circuit as set forth in claim 11, wherein:

the target element is a spiral inductor.

13. The integrated circuit as set forth in claim 1, wherein:

the metal fence is grounded.

14. The integrated circuit as set forth in claim 1, wherein:

a distance SF between the metal fence and the target element is given by SF>25μm.

15. The integrated circuit as set forth in claim 1, wherein:

the metal fence is AlCu;

a thickness of each metal wire layer of the metal fence is 0.6μm to 1.5μm; and

the WF is given by WF>5μm.

16. The integrated circuit as set forth in claim 1, wherein:

a height of the metal fence as a whole is equal to or higher than a level of the target element.

17. The integrated circuit as set forth in claim 1, wherein:

a top and a bottom of the target element are not covered with the metal fence, so that the top and the bottom of the target element are exposed.